



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,513	10/03/2003	Werner Juengling	MI22-2391	1971
21567	7590	06/26/2006	[REDACTED]	EXAMINER
WELLS ST. JOHN P.S. 601 W. FIRST AVENUE, SUITE 1300 SPOKANE, WA 99201			[REDACTED]	KEBEDE, BROOK
			[REDACTED]	ART UNIT
			[REDACTED]	PAPER NUMBER
				2823

DATE MAILED: 06/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/678,513	JUENGLING, WERNER	
	<b>Examiner</b>	<b>Art Unit</b>	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 4/10/06.
- 2a) This action is **FINAL**.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 40-70 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) 40-47 and 51-55 is/are allowed.
- 6) Claim(s) 48-50,56,57,59-61 and 64-67 is/are rejected.
- 7) Claim(s) 58,62,63 and 68-70 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____ .  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>4/10/06</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____ .                                  |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 10, 206 has been entered.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 48, 50, 56, 57, 59 - 61, and 64 – 67 are rejected under 35 U.S.C. 102(e) as being anticipated by Jeng et al. (US/5,994,228).**

Re claim 48, Jeng et al. disclose a semiconductor processing method comprising: forming a conductive line (117 119) (i.e., polysilicon gate line) over a substrate (100), the conductive line (117) having a conductive portion (see Fig. 3) and silicon nitride material (121) over the conductive portion (117), and silicon oxide material (131) over the silicon nitride material (131) (see Fig. 3b) forming encapsulation material (132 133) over the conductive line (117); and in a common masking step (140) (see Fig. 3d), etching a doping

Art Unit: 2823

window opening (170) over a substrate (100) active area adjacent the conductive line (117) and removing at least some of the encapsulation material (130) over the conductive line (117 119) and some of the silicon nitride material (121) over the conductive portion (117 119) of the conductive line (117) to form contact opening (160) to the conductive line (117) (see Figs. 3a – 3f; and related text in Col. 5, line 25 – Col. 6, line 67).

Re claim 50, Jeng et al. disclose a semiconductor processing method comprising: forming a conductive word line (117) over a substrate (100); forming a silicon nitride layer (121) over the word line (117); forming a silicon oxide layer (131) over the silicon nitride layer (121) (see Figs. 3b and 3c); forming encapsulation material (132 133) over the silicon oxide layer (131), the silicon nitride layer (121) and the conductive word-line (117); the encapsulation material forming sidewall spacers (123) over the conductive word-line (117) selectively removing at least some of the encapsulation material (see Fig. 3d) relative to the silicon oxide layer (131); and selectively removing at least some of the silicon oxide layer relative to the layer wherein the selectively removing forms at least part of a silicon nitride contact opening over the word line (117) (see Figs. 3a – 3f; and related text in Col. 5, line 25 – Col. 6, line 67).

Re claim 56, as applied to claim 48 above, Jeng et al. disclose all the claimed limitations including wherein the etching of the doping window opening comprises forming a pair of doping window openings (33 34) adjacent opposite sides of the conductive line (see Figs. 3a – 3f; and related text in Col. 5, line 25 – Col. 6, line 67).

Re claim 57, as applied to claim 48 above, Jeng et al. disclose all the claimed limitations including wherein the etching comprises exposing the conductive portion of the conductive line (see Figs. 3a – 3f; and related text in Col. 5, line 25 – Col. 6, line 67).

Re claim 59, as applied to claim 48 above, Jeng et al. disclose all the claimed limitations including wherein the encapsulation material comprises material other than oxide (see Figs. 3a – 3f; and related text in Col. 5, line 25 – Col. 6, line 67).

Re claim 60, as applied to claim 48 above, Jeng et al. disclose all the claimed limitations including wherein the forming of the encapsulation material comprises forming after the forming of the conductive line (see Figs. 3a – 3f; and related text in Col. 5, line 25 – Col. 6, line 67).

Re claim 61, as applied to claim 48 above, Jeng et al. disclose all the claimed limitations including wherein the encapsulation material and the silicon oxide material comprise different materials (see Figs. 3a – 3f; and related text in Col. 5, line 25 – Col. 6, line 67).

Re claim 64, as applied to claim 48 above, Jeng et al. disclose all the claimed limitations including wherein the encapsulation material and silicon oxide material are separate and distinct (see Figs. 3a – 3f; and related text in Col. 5, line 25 – Col. 6, line 67).

Re claim 65, as applied to claim 48 above, Jeng et al. disclose all the claimed limitations including wherein the forming of the conductive line having the silicon oxide material comprises a first forming step, and wherein the forming of the encapsulation material comprises a second forming step which is distinct and separate from the first forming step (see Figs. 3a – 3f; and related text in Col. 5, line 25 – Col. 6, line 67).

Re claim 66, as applied to claim 48 above, Jeng et al. disclose all the claimed limitations including wherein the forming of the conductive line having the silicon oxide material comprises a forming step performed in a first time period, and wherein the forming of the encapsulation material comprises a forming step performed in a second time period which is different from the first time period (see Figs. 3a – 3f; and related text in Col. 5, line 25 – Col. 6, line 67).

Re claim 67, as applied to claim 48 above, Jeng et al. disclose all the claimed limitations including wherein the forming of the conductive line having the silicon oxide material comprises a forming step that is entirely completed before the forming of the encapsulation material (see Figs. 3a – 3f; and related text in Col. 5, line 25 – Col. 6, line 67).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. **Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeng et al. (US/5,994,228), as applied in Paragraph 3 above, in view of Dennison (US/5,637,525).**

Re claim 49, as applied to claim 48 in Paragraph 3 above, Jeng et al. disclose all the claimed limitations. Although it is obvious, i.e., from the Jeng et al. disclosure, Jeng et al. do not specifically disclose gas diffusion doing through the doping window opening into the substrate.

Dennison discloses all the claimed limitations including gas diffusion doing through the doping window opening into the substrate (see Figs. 8 and 9) in order to enhance the impurity concentration in the substrate and thereby providing source drain contact region for the PMOS or NMOS transistor regions (see Col. 4, line 65 – Col. 5, line 18).

Both Jeng et al. and Dennison teachings are directed to fabricating of MOSFET device that includes forming source/drain contact and gate contact. Therefore, the teachings of Jeng et al. and Dennison are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Jeng et al. reference with gas diffusion doing though the doping window opening into the substrate as taught by Dennison in order to enhance the impurity concentration in the substrate and thereby providing source drain contact region for the PMOS or NMOS transistor regions

*Allowable Subject Matter*

6. Claims 40-47 and 51-55 allowed over prior art of record.
7. Claims 58, 62, 63, 68, 69 and 70 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

*Response to Arguments*

8. Applicant's arguments with respect to claims 48 -50, 56, 57, 59 - 61, and 64 – 67 have been considered but are moot in view of the new ground(s) of rejection.
9. Applicant's arguments, with respect to the rejection of claims 58 and 62 under 35 U.S.C. § 112, first Paragraph have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

*Conclusion*

10. **THIS ACTION IS MADE NON-FINAL.**

*Correspondence*

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

*Brook Kebede*  
Brook Kebede  
Primary Examiner  
Art Unit 2823

BK  
June 22, 2006